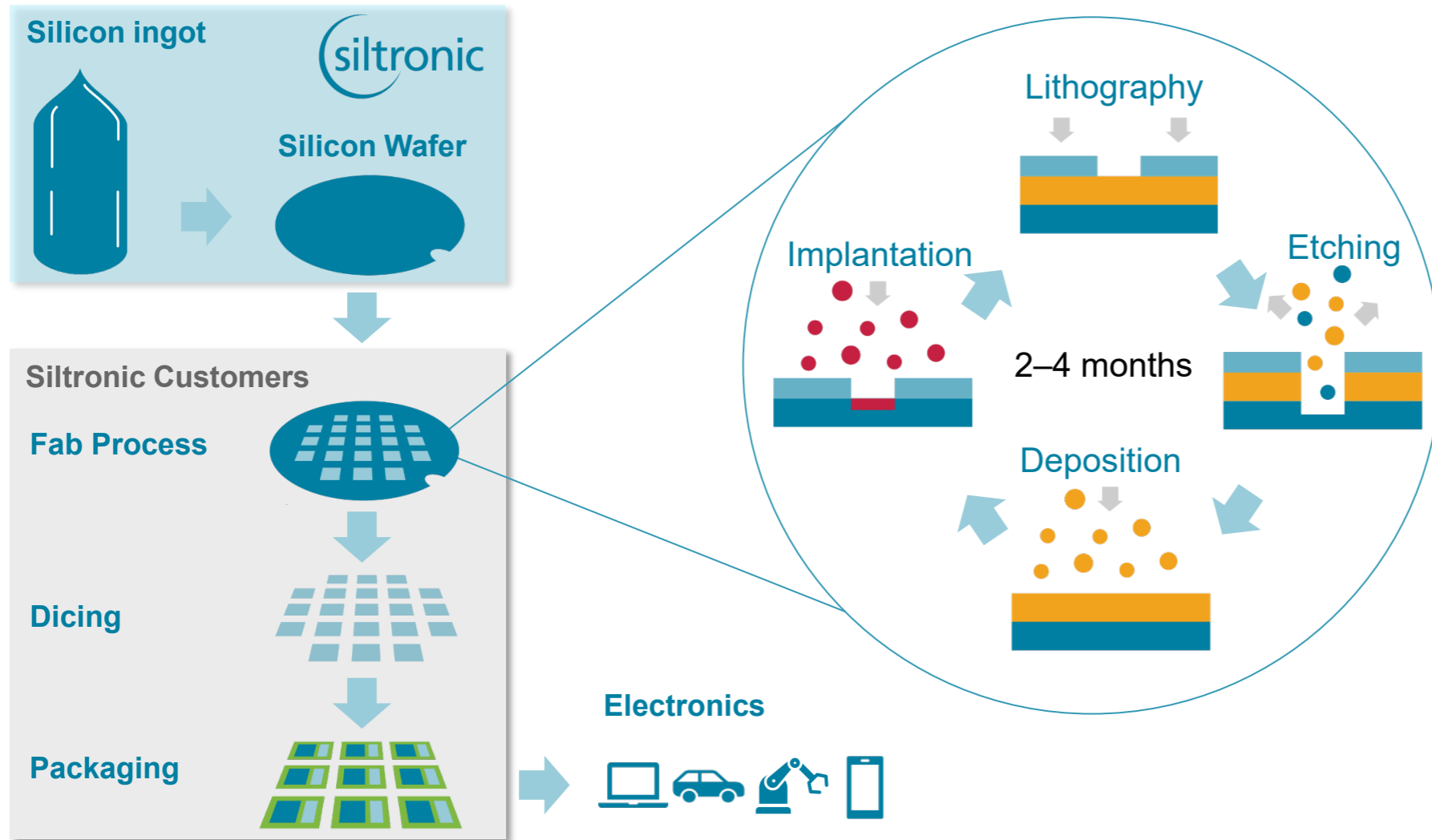


VALUE GENERATION THROUGH INNOVATION AND TECHNOLOGY

Dr. Christian Parthey
VP Application Technology
November 30, 2023

SILICON WAFERS FUEL ELECTRONICS WITH SILTRONIC AS A KEY PLAYER



6 months+

from the ingot to the end product



99%

of the semiconductor market is based on silicon



>90 million

300 mm wafers processed in 2022

OUR WAFERS ARE A HIGH-TECH PRODUCT WHERE A SINGLE NANOMETER MAKES THE DIFFERENCE

Macroscopic Description

Diameter and notch position

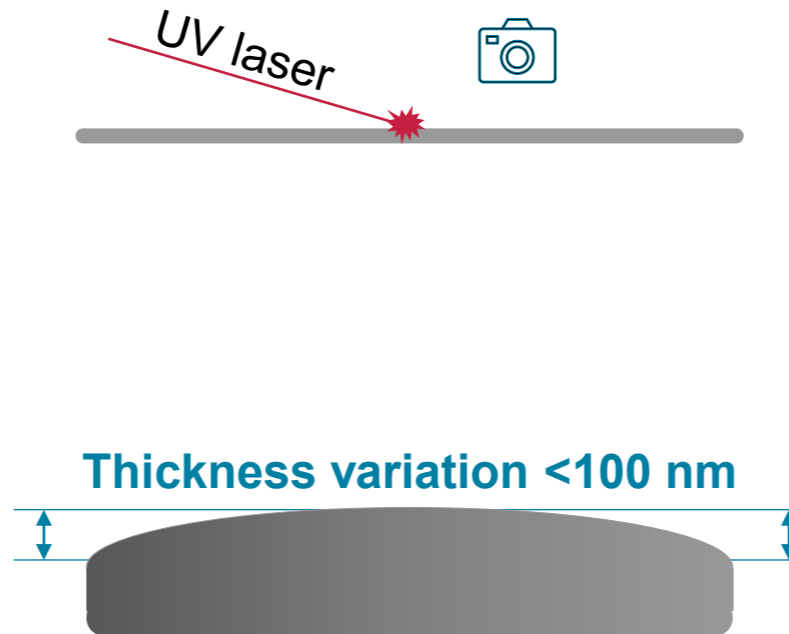


Edge profile



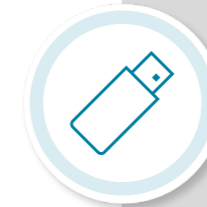
Control Parameters

Maximum number of particles



Up to 55

measurements per wafer



>5 GB

of data are generated per wafer



AI analysis

and statistics are the key for high-tech mass production


SILTRONIC'S PRODUCT PORTFOLIO COVERS ALL SEMICONDUCTOR SEGMENTS

Logic devices

Memory devices

Power devices


CRYSTAL


 Leading Edge
Trailing Edge

 Leading Edge

Ω Low resistivity
 O_2 Low oxygen


POLISHED
WAFER

 Leading Edge
Trailing Edge

 Leading Edge

Trailing Edge

EPI LAYER

 Leading Edge
Trailing Edge

Trailing Edge



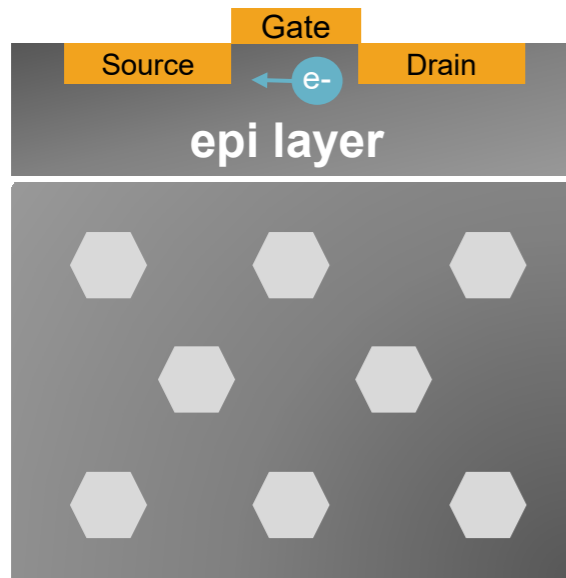
WE CONTROL AND TAILOR DIFFERENT CRYSTAL PROPERTIES FOR SPECIFIC CUSTOMER NEEDS

Wafers for

Logic devices

In a Logic wafer, electrons only travel in the epi layer close to the surface

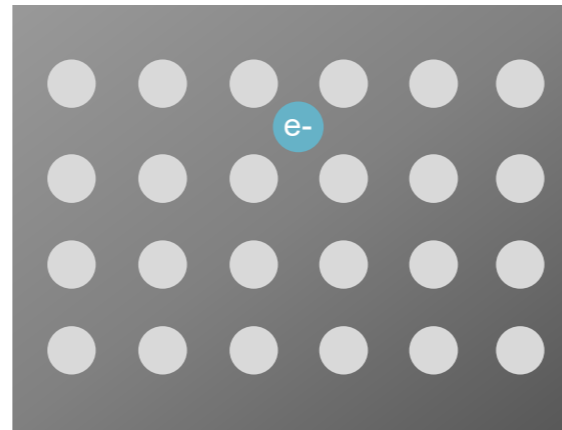
Requirement: high quality epi layer & engineered substrate wafer



Memory devices

In a Memory wafer electrons are stored in cells

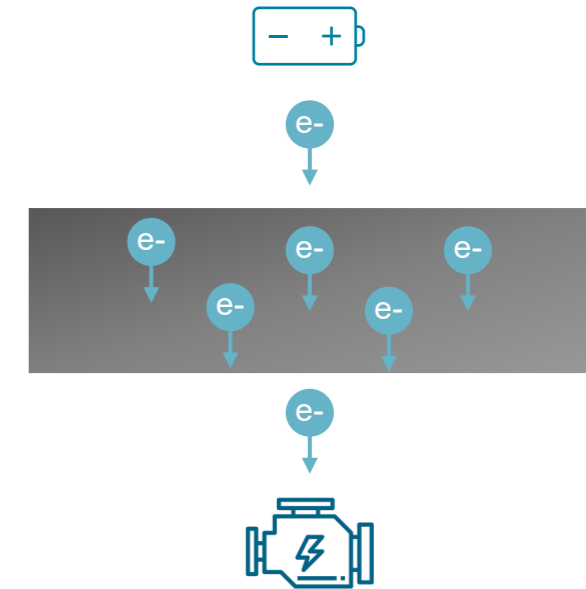
Requirement: high quality crystal and well controlled flatness all the way to the wafer edge



Power devices

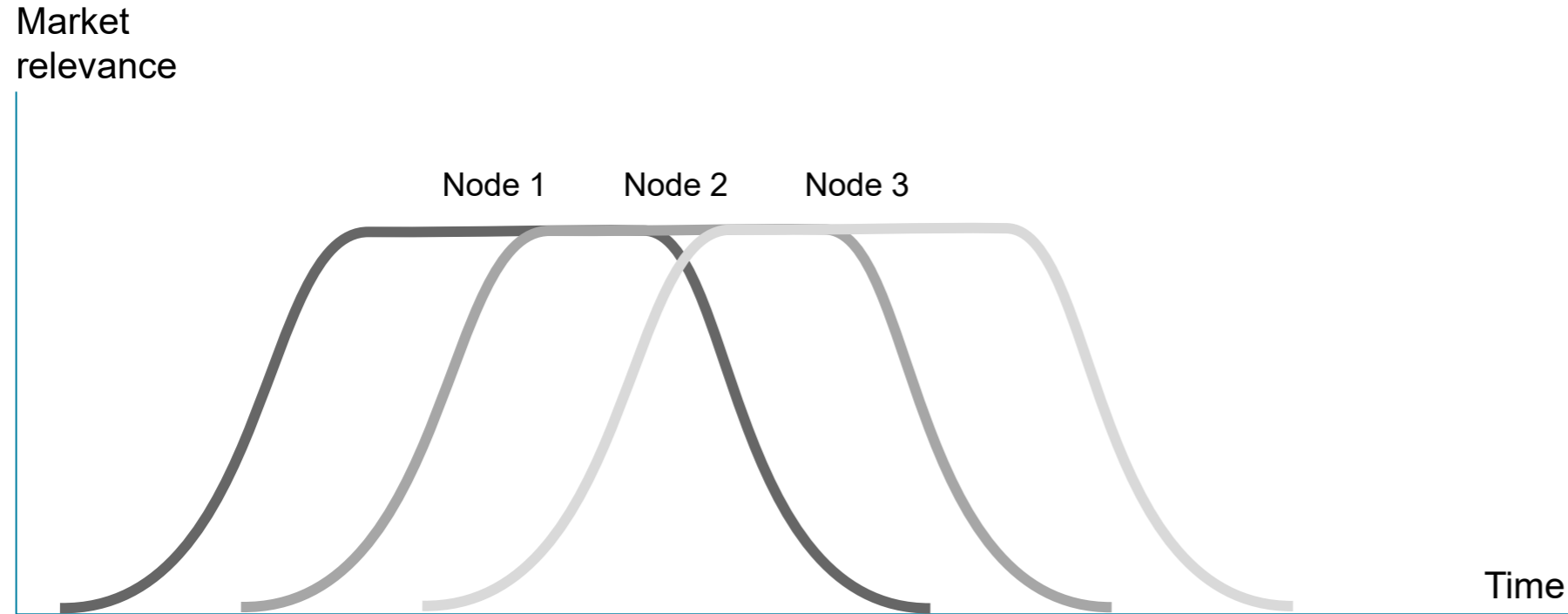
In a wafer for high Power use, the current flows through the bulk

Requirement: low resistivity



MOORE'S LAW IS DRIVING THE INDUSTRY AND INNOVATION CYCLES

Semiconductor technology nodes' life-cycle (schematic)



Moore's Law:

The number of transistors on a microchip doubles every two years.



Moore's Law

is the semiconductor industry's pace maker



Two years

cadence to introduce new technology nodes

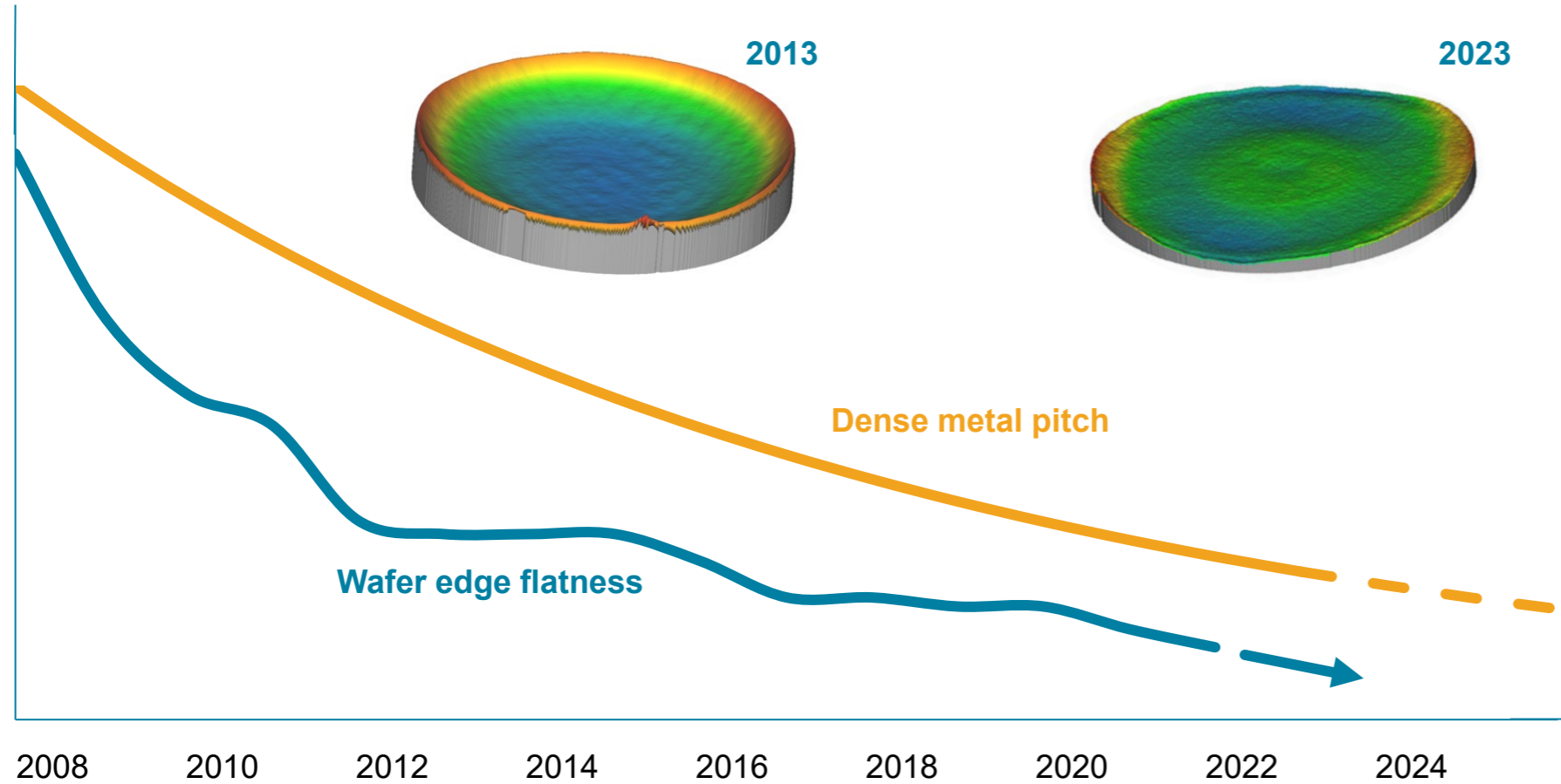


Functionality

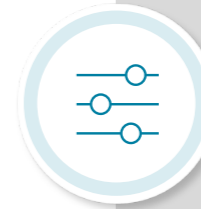
gains at price parity drive continued demand

SEMICONDUCTOR DEVICES IMPROVE AND SILICON WAFERS HAVE TO STAY AHEAD

Wafer edge flatness in nm



Source: Siltronic estimate based on ASML and IRDS 2022



Flatness

controlled down to 10 nm locally



Finish

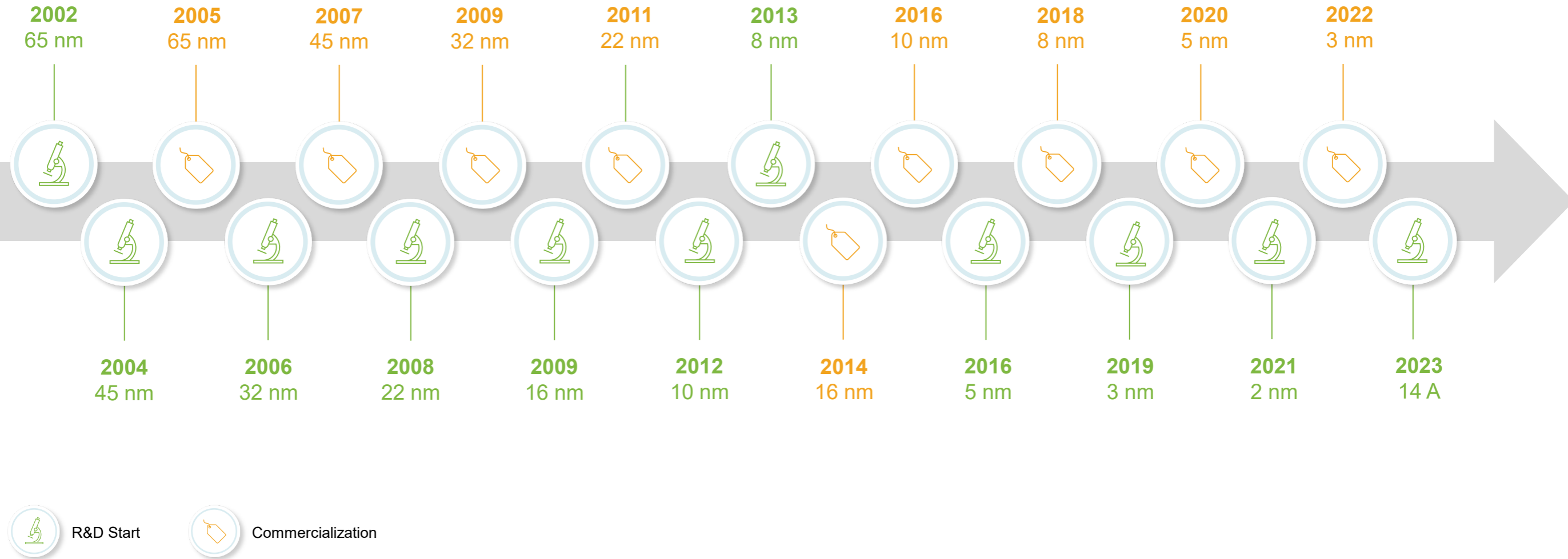
control of particles down to 14 nm in size



Purity

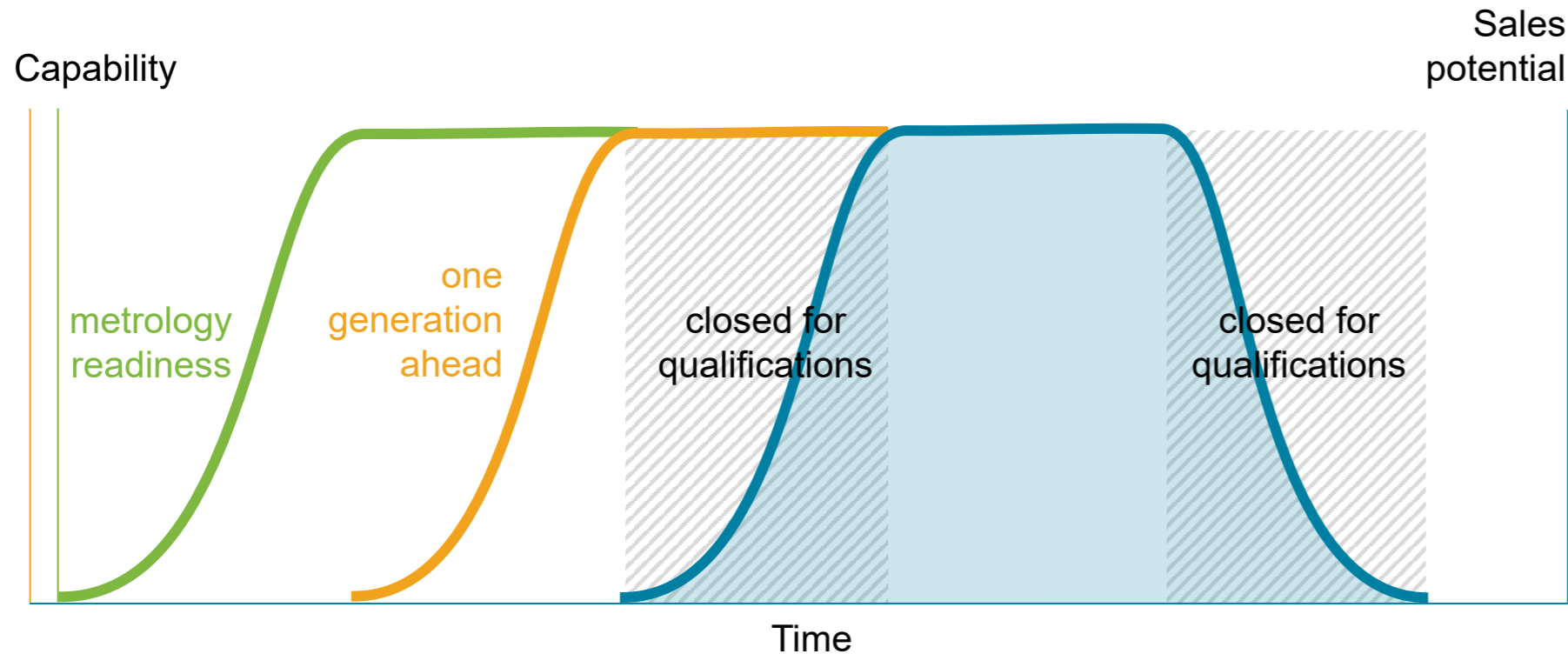
>99.99999% silicon to grow a crystal

SILTRONIC HAS STAYED AHEAD OF THE CURVE AS A LEADING EDGE PLAYER FOR DECADES



FAST DEVELOPMENT ALLOWS TO CAPTURE THE FULL SALES POTENTIAL OF A NODE

Impact of Leading Edge strategy on generated sales (schematic)



Start early
Innovate fast



Excellent customer relationship
High R&D resources



Price

premium for Leading Edge



Profitability

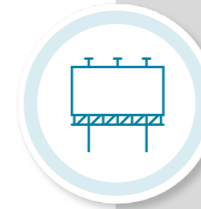
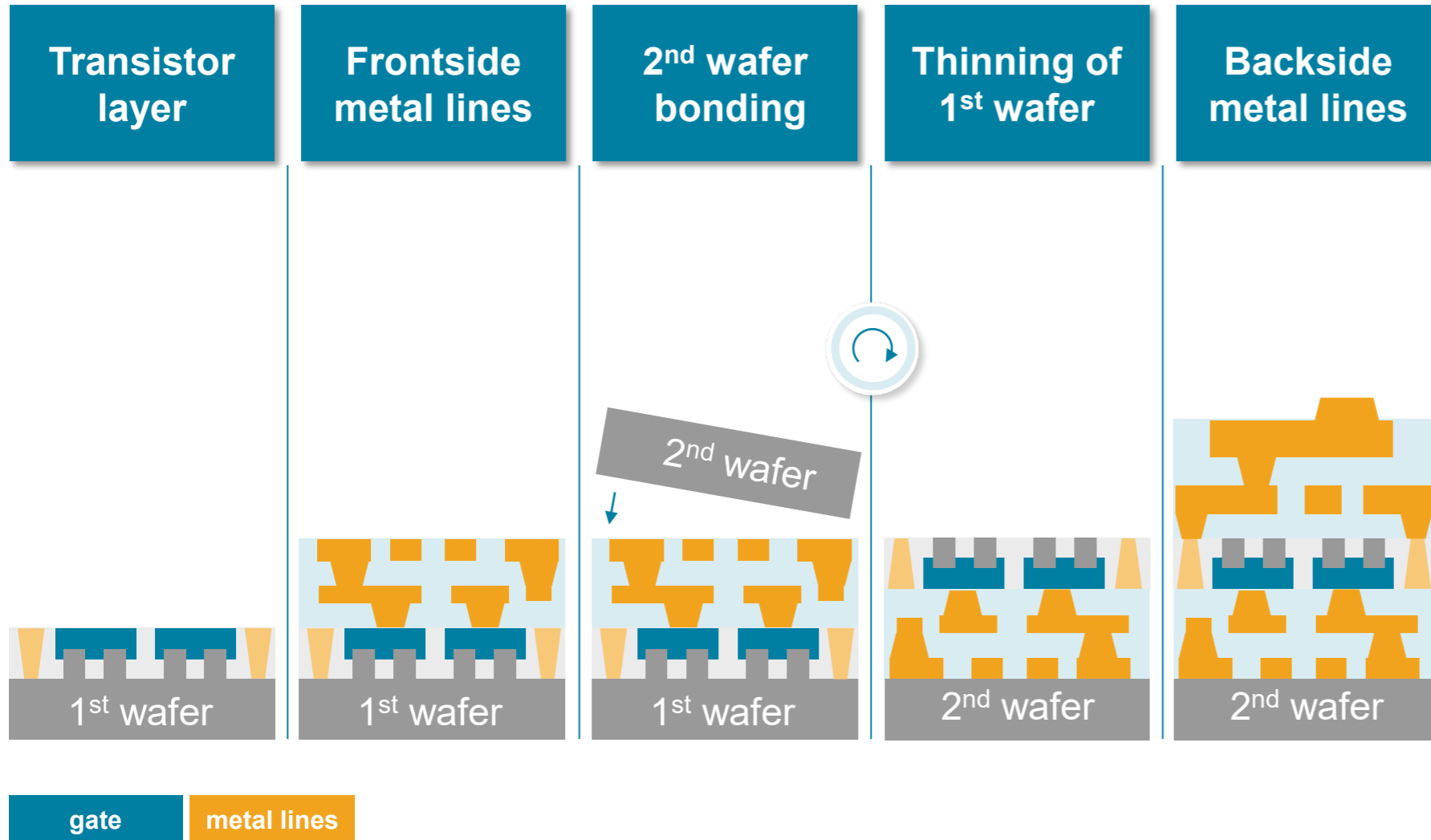
higher for Leading Edge



5–6%

of sales invested in R&D

A14 LOGIC NODE REQUIRES BACKSIDE POWER DELIVERY WITH A NEW WAFER PRODUCT



2024

projected year of volume ramp



>4 years

ago we started development



Advanced

flatness control is one of the key enablers

Source: Siltronic based on SemiWiki and Luc Van den Hove, IMEC, Future Summits 2022

KEY TAKEAWAYS

We **anticipate our customers' needs** and develop our wafers accordingly

Our technology leadership allows **growth in all segments:** Memory, Logic, and Power



We have a **proven track record** in fulfilling our customers' requirements on time

We will stay ahead of the innovation curve by keeping our **R&D focus**

QUESTIONS?



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